

CCA

MR-58P

33	* A82X
34	* A84X
35	* A87X
36	* A89X
37	* A18X
38	* A13X
39	* A16X
40	* BAUDR
41	* CLK8
42	* -15V
43	* 24V
44	* EXFDT
45	* D82X
46	* D85X
47	
48	
49	
50	

01	* A81X
02	* A83X
03	* A86X
04	* A88X
05	* A11X
06	* A14X
07	* 8V
08	* 8V
09	* 8V
10	* +5V
11	* +5V
12	* +5V
13	* 081X
14	* 084X
15	* 086X
16	
17	
18	

CCX1

MR-58P

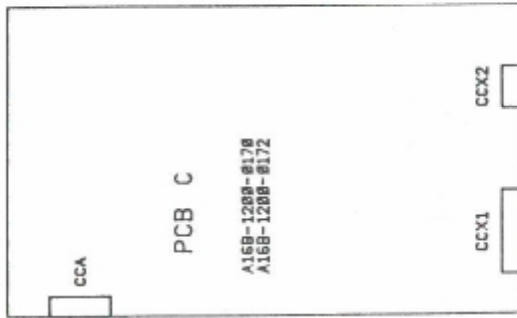
33	RS
34	CS
35	DR
36	OV
37	* CD
38	* OV
39	* OV
40	* SD
41	* RD
42	* OV
43	ER
44	
45	
46	SD
47	OV
48	CH89
49	PI
50	FG

01	TTY1
02	TTY2
03	TTY3
04	OV
05	
06	
07	PR
08	TE
09	ERR
10	* 6V
11	CH01
12	CH02
13	CH03
14	CH04
15	CH05
16	CH06
17	CH07
18	CH08

CCX2

MR-28P

14	CLKINH
15	EXCLKI
16	DTC2
17	EXCLKO
18	* 6012IH
19	
20	FG
08	8V
09	8V
10	8V
11	8V
12	8V
13	
01	VIDEO
02	HSYNC
03	VSYNC
04	
05	
06	
07	



C15

DSUB-25S

01	FG
02	* SD
03	* RD
04	RS
05	CS
06	DR
07	OV
08	* CD
09	
10	
11	
12	
13	
14	
15	
16	
17	
18	
19	
20	
21	
22	
23	
24	
25	* 24V

C14

MR-28P

14	CH4
15	CH5
16	CH6
17	CH7
18	CH8
19	CH9
20	PI
08	FG
09	SD
10	OV
11	CH1
12	CH2
13	CH3
01	PR
02	TE
03	ERR
04	TTY3
05	* 6V
06	TTY2
07	TTY1

ASR33.FACIT4878 INTERFACE

TO CRTGRAPHIC DISPLAY UNIT

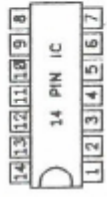
RS-232C INTERFACE

CG00

GRAPHIC/PUNCHER INTERFACE

A16C-1200-0170/05

FANUC LTD
AWI-434960



AWI-434961

MAIN CPU DI/DO (SYSTEM 6)

#E7EE	(01)	D7	CRT/P	D6	GRC/P	D5	14/9	D4	IRM	D3	DO6	D2	CR9	D1	FACIT	D0
* CRT/P ---- = 1/1 * WITH CRT/PUNCH CONTROL P.C.B. * GRC/P ---- = 1/1 * WITH GRAPHIC/PUNCH CONTROL P.C.B. FACIT ---- = 1/1 * FACIT 487B IS CONNECTED. IRM ---- = 1/1 * INPUT READY (IFIFO IS NOT FULL.) DO6 ---- GRAPHIC CPU DO CR9 ---- = 1/1 * WITH 9 INCH CRT = 1/1 * WITH 12 INCH CRT 14/9 ---- = 1/1 * WITH 12 INCH CRT = 1/1 * WITH 9 OR 12 INCH CRT																
#E7FB	(01/DO)	D7	P6	D6	P5	D5	P4	D4	P3	D3	P2	D2	P1	D1	P0	D0
P8-P7 --- ASR33A-RS-232C DATA(DI/DO) FACIT 487B DATA(DO)																

#E7F2	(01/DO)	D7	S6	D6	S5	D5	S4	D4	S3	D3	S2	D2	S1	D1	S0	D0
ERR TE PB PI																

58-57 --- ASR-RS-232C STATUS(DI/DO)
 ERR ---- = 1/1 * ERROR OF FACIT 487B SIDE
 TE ---- = 1/1 * PAPER TAPE END (FACIT 487B)
 PB ---- = 1/1 * PUNCH BUSY (FACIT 487B)
 PI ---- PUNCH INSTRUCTION (FACIT 487B)

#E7F4	(00)	D7	CLDCD	D6	PINH	D5	FA/ASRS	D4	RS/AS	D3	D2	D1	D0
CLDCD ---- = 1/1 * CLEAR DCD HOLD SIGNAL PINH ---- = 1/1 * PUNCH INHIBIT													

FA/ASRS,RS/AS	FACIT 487B	ASR33	RS-232C
FA/ASRS	1	0	0
RS/AS	0	1	1

SY3 ---- = 1/1 * SYSTEM 3 = 1/1 * SYSTEM 6
 5MHZ ---- = 1/1 * MAIN CLOCK FREQ. IS 5MHZ.

#E7F5	(01)	D7	D6	D5	D4	D3	D2	D1	D0
DCD ---- = 1/1 * DATA (FROM RS-232C INTERFACE) IS NOT GOOD.									

#E7FC	(01/DO)	D7	GC07	D6	GC06	D5	GC05	D4	GC04	D3	GC03	D2	GC02	D1	GC01	D0
GC08- ---- DO MAIN CPU --> GRAPHIC CPU																

MAIN CPU DI/DO (SYSTEM 3)

#E7EC	(01)	D7	D6	D5	D4	D3	D2	D1	D0
* GRC/P ---- = 1/1 * WITH GRAPHIC/PUNCH CONTROL P.C.B.									
#E7F4	(08)	D7	D6	D5	D4	D3	D2	D1	D0
SY3 ---- = 1/1 * SYSTEM 3 = 1/1 * SYSTEM 6									
#E7F6	(01)	D7	D6	D5	D4	D3	D2	D1	D0
* IRM ---- = 1/1 * INPUT READY (IFIFO IS NOT FULL) * DO6 ---- GRAPHIC CPU DO									

#E7FC	(01/DO)	D7	GC07	D6	GC06	D5	GC05	D4	GC04	D3	GC03	D2	GC02	D1	GC01	D0
GC08- ---- DO MAIN CPU --> GRAPHIC CPU																

CG01

DATE													
DES	CHK	INS	CHK	DES	CHK	DES	CHK	DES	CHK	DES	CHK	DES	CHK
PART NO. A16C-1200-0170/05 FANUC LTD AWI-434961													

GRAPHIC CPU DI/DO

PORT 1 (DI/DO) 07 =CR9 06 TSM 05 DISMD 04 COK 03 GOK 02 =S1B/8 01 IR6 =CR9/12

- * CR9 --- 1/8" 9 INCH CRT MODE(DO)
- TSM --- 1/8" TRI SIZE MODE(DO)
- DISMD --- 1/8" DISPLAY MODE(DO)
- COK --- 1/8" CHAR. DISPLAY ENABLE(DO)
- GOK --- 1/8" GRAPHIC DISPLAY ENABLE(DO)
- S1B/8 --- 1/8" 1B DOTS/CHAR.(DO)
- * CR9/12 --- 1/8" WITH 9 INCH CRT(DI)
- IR6 --- 1/8" INPUT READY(FIFO IS NOT FULL) (DI)

PORT 3 (DI/DO) 07 1(RD) 06 1(WR) 05 ORG 04 3(INT) 03 2(INT) 02 DOG 01 D18

- ORG --- 1/8" OUTPUT READY (FIFO IS NOT EMPTY) (DI)
- DOG --- GRAPHIC CPU DO

6808-5FFF A88-8 (DO) 07 06 05 04 03 02 01 D18

NOTE 1 RAB-RA4 --- REGISTER ADDRESS FOR CRTC

A88-1 (DO) 07 RD7 06 RD6 05 RD5 04 RD4 03 RD3 02 RD2 01 RD1 018 RD0

RDB-RD7 --- REGISTER DATA FOR CRTC

NOTE 1 8118 XXXX XXXX XXXX
8118 XXXX XXXX XXXX
DON'T CARE

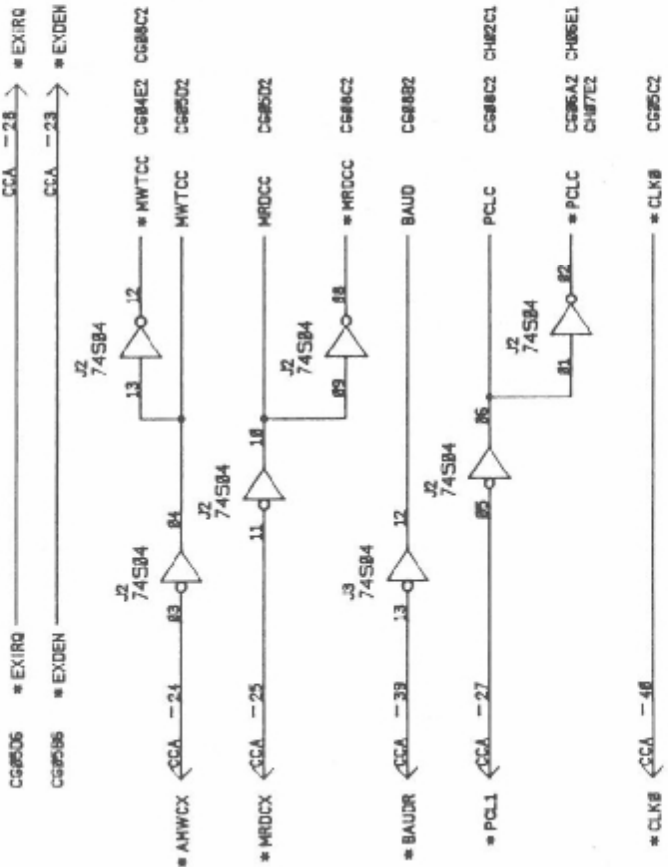
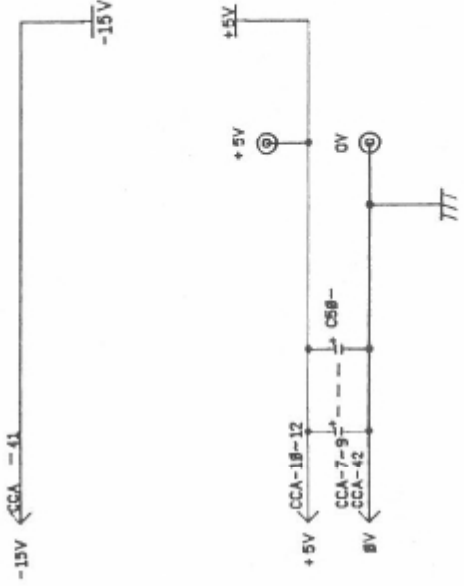
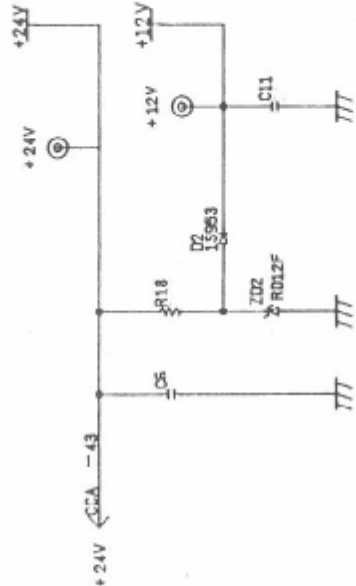
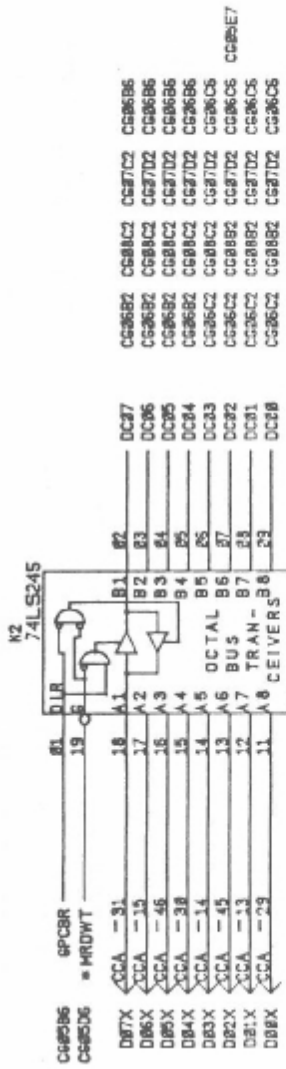
7828-7FFF (DI/DO) 07 06 05 04 03 02 01 D18

6C07 6C06 6C05 6C04 6C03 6C02 6C01 6C08

NOTE 2 6C08- --- DI MAIN CPU → GRAPHIC CPU

NOTE 2 8111 XXXX XXXX XXXX
DON'T CARE

CG02									
REV	DATE	BY	CHKD	DATE	BY	CHKD	DATE	BY	CHKD
PART NO. A16C-1200-0170/05									
FANUC LTD 083 /									
AWI-434962									



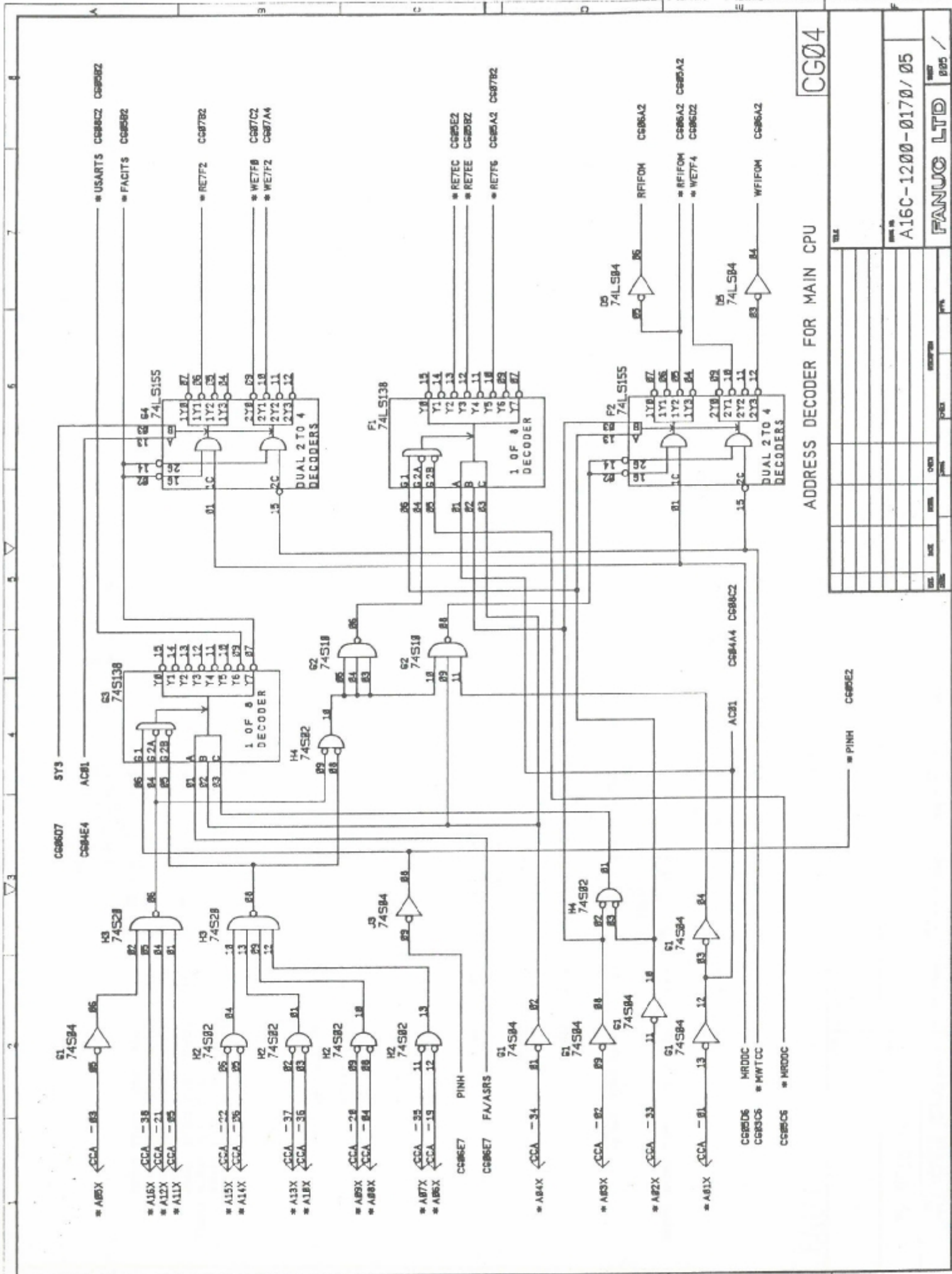
CG03

MAIN CPU INTERFACE

NO.	NAME	TYPE	VALUE
1	RES	RES	10K
2	RES	RES	10K
3	RES	RES	10K
4	RES	RES	10K
5	RES	RES	10K
6	RES	RES	10K
7	RES	RES	10K
8	RES	RES	10K
9	RES	RES	10K
10	RES	RES	10K
11	RES	RES	10K
12	RES	RES	10K
13	RES	RES	10K
14	RES	RES	10K
15	RES	RES	10K
16	RES	RES	10K
17	RES	RES	10K
18	RES	RES	10K
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26	RES	RES	10K
27	RES	RES	10K
28	RES	RES	10K
29	RES	RES	10K
30	RES	RES	10K
31	RES	RES	10K
32	RES	RES	10K
33	RES	RES	10K
34	RES	RES	10K
35	RES	RES	10K
36	RES	RES	10K
37	RES	RES	10K
38	RES	RES	10K
39	RES	RES	10K
40	RES	RES	10K
41	RES	RES	10K
42	RES	RES	10K
43	RES	RES	10K
44	RES	RES	10K
45	RES	RES	10K
46	RES	RES	10K
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51	RES	RES	10K
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55	RES	RES	10K
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59	RES	RES	10K
60	RES	RES	10K
61	RES	RES	10K
62	RES	RES	10K
63	RES	RES	10K
64	RES	RES	10K
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66	RES	RES	10K
67	RES	RES	10K
68	RES	RES	10K
69	RES	RES	10K
70	RES	RES	10K
71	RES	RES	10K
72	RES	RES	10K
73	RES	RES	10K
74	RES	RES	10K
75	RES	RES	10K
76	RES	RES	10K
77	RES	RES	10K
78	RES	RES	10K
79	RES	RES	10K
80	RES	RES	10K
81	RES	RES	10K
82	RES	RES	10K
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84	RES	RES	10K
85	RES	RES	10K
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87	RES	RES	10K
88	RES	RES	10K
89	RES	RES	10K
90	RES	RES	10K
91	RES	RES	10K
92	RES	RES	10K
93	RES	RES	10K
94	RES	RES	10K
95	RES	RES	10K
96	RES	RES	10K
97	RES	RES	10K
98	RES	RES	10K
99	RES	RES	10K
100	RES	RES	10K

AW1-1200-0170/05
 FANUG LTD
 AW1-434963

ADDRESS DECODER FOR MAIN CPU



REV	DATE	BY	CHK	APP	REV	DATE	BY	CHK	APP	REV	DATE	BY	CHK	APP	REV	DATE	BY	CHK	APP	

PART NO		A16C-1200-0170/05	
FANUC LTD		AWI-434964	

AW1-434965

HWDCU05

85

The schematic diagram illustrates the DATA BUS GATE CONTROL circuit. It is organized into a grid with columns labeled A through F and rows labeled 1 through 6. The circuit includes a central HEX 0-TYPE FLIP-FLOPS (74LS174) and a 3-STATE BUFFERS (74LS367). Various logic gates (AND, OR, NOT) and inverters (74LS04) are used to process control signals. The signals are as follows:

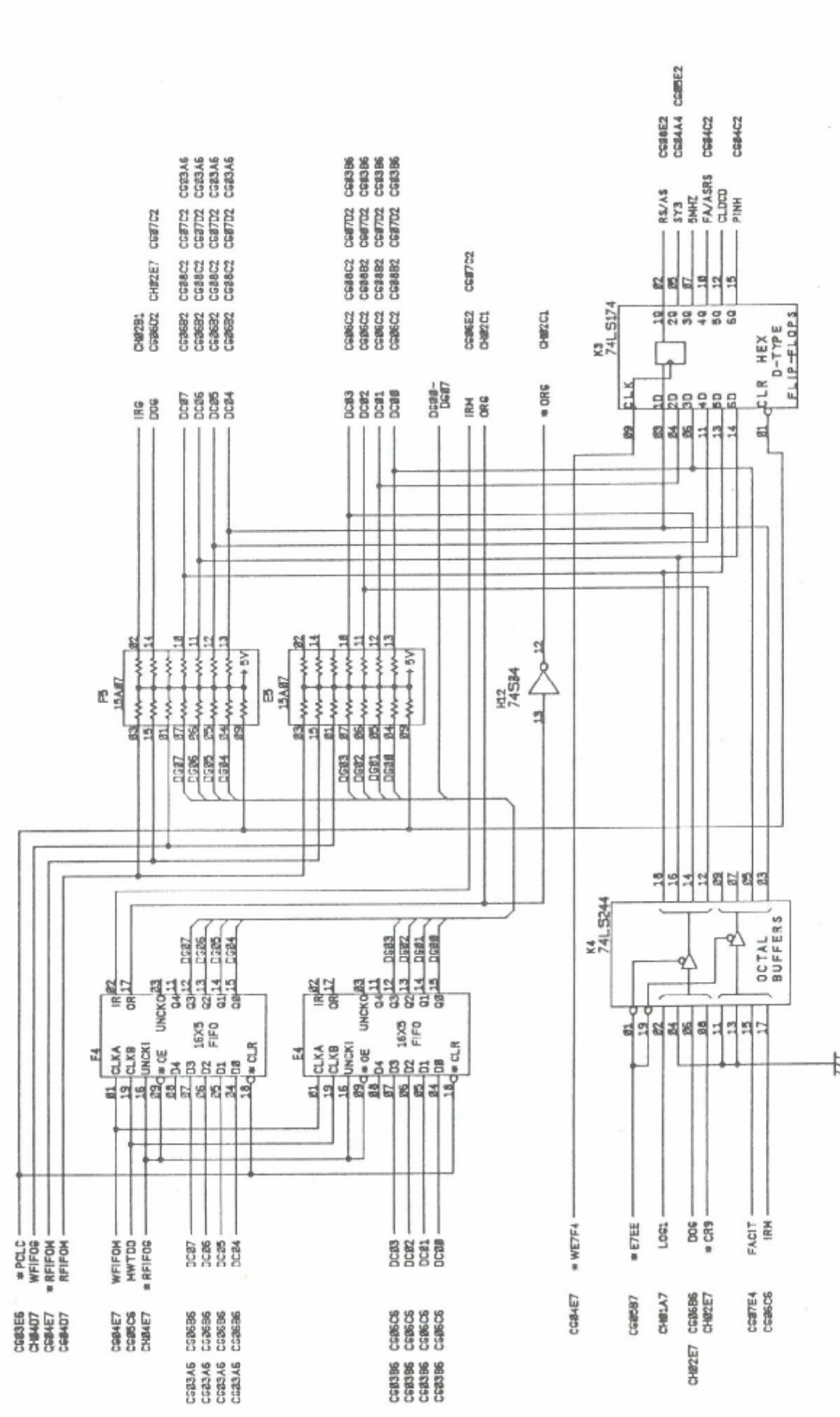
- Row 1:**
 - Column A: C684D7, C684E7, C684A7, C684A7, C685C6
 - Column B: C684C7
 - Column C: C683E6, C683E6, C688A6, C683C5, C683C5
 - Column D: C684F4
 - Column E: C684C7, C686D7
- Row 2:**
 - Column A: RE7F6, RFIFOM, USARTS, FACITS, MRDCC
 - Column B: RE7EE
 - Column C: CLK, PCLC, RXRDY, MRDCC, MWTC
 - Column D: PINH
 - Column E: RE7EC, SY3
- Row 3:**
 - Column A: EXDEN
 - Column B: CPCBP
 - Column C: MRDCC, MRDCC, MRDWT
 - Column D: EXIRO
- Row 4:**
 - Column B: E7EE
 - Column C: HWTDO
 - Column D: MRDWT
- Row 5:**
 - Column B: DB2X
- Row 6:**
 - Column B: DB2X

The circuit also includes several logic gates and inverters, such as 74LS04, 74LS08, 74LS32, 74LS174, and 74LS367. The 3-STATE BUFFERS (74LS367) are connected to the output of the flip-flops and provide a 3-state output to the data bus.

CG05

DATA BUS GATE CONTROL

AW1-434965
 PART NO. A16C-1200-0170/05
 FANUC LTD
 826 /



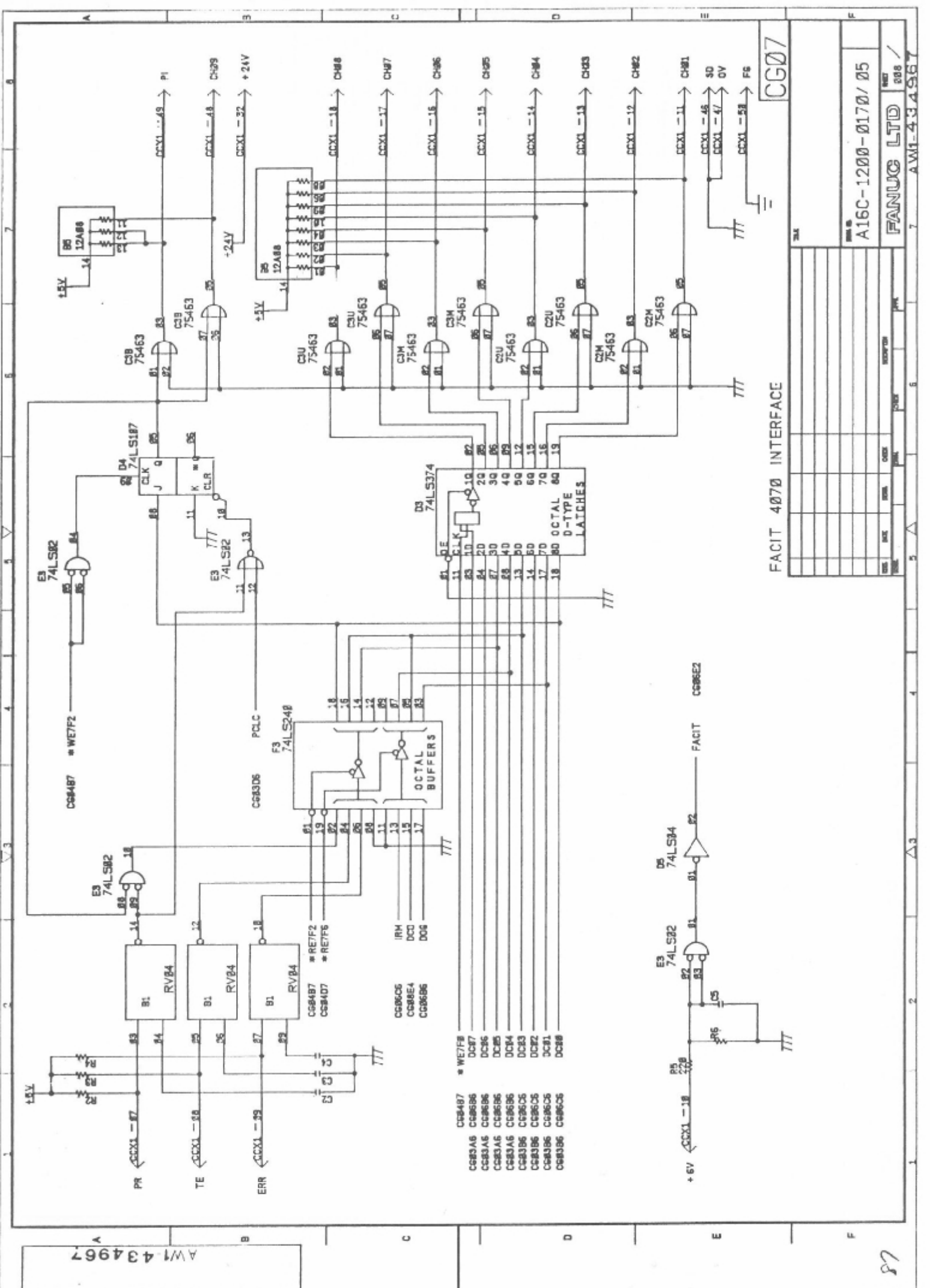
CG06

FIFO

REV	DATE	BY	CHKD	APPR	DESCRIPTION

NOTE
DCB0-DCB7 CH202 CH204 CH206 CH207 CH208

AWI-1200-0170/05
FANUC LTD
REV 007 /



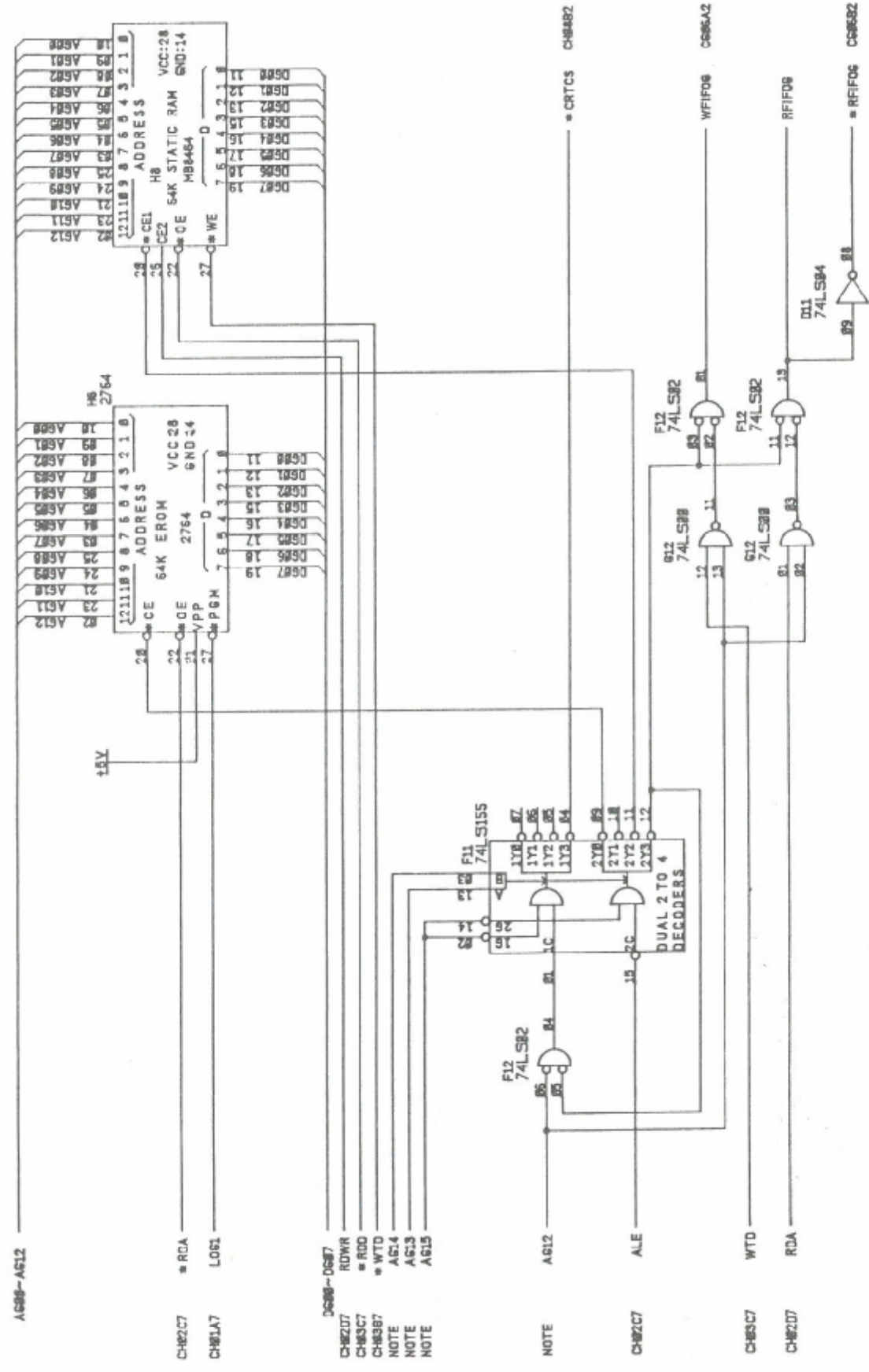
FACIT 4070 INTERFACE

CG07

REV	DATE	BY	CHKD	REVISION

AWI-434967
 PART NO. A16C-1200-0170/05
 FANUC LTD
 REV 006 /

AWI-434967



EROM . WORK RAM

CH04

NO.	DATE	REV.	BY	CHKD.	APPV.

AW1-434972
 A16C-1200-0170/05
 FANUC LTD
 813 /

NOTE
 AG12 C185 C186 C188 C187
 D688-D687 C186 C187 C188 C185 C182

AWI-434973

93

NOTE
 CH888-CH812
 RA888-RA83
 MA888-MA11
 AG888-AG15

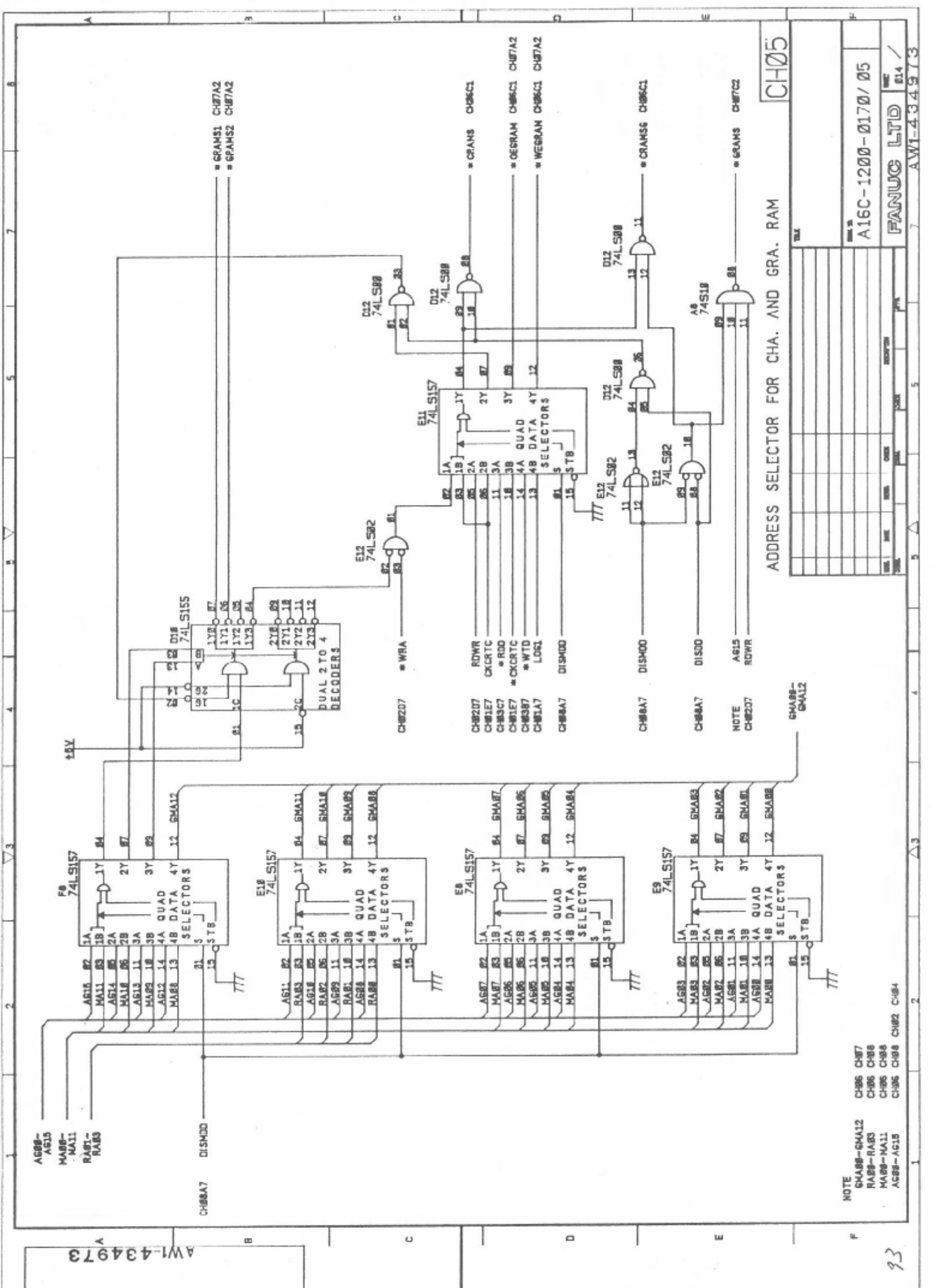
CH887
 CH886
 CH885
 CH884
 CH883
 CH882
 CH881

ADDRESS SELECTOR FOR CHA. AND GRA. RAM

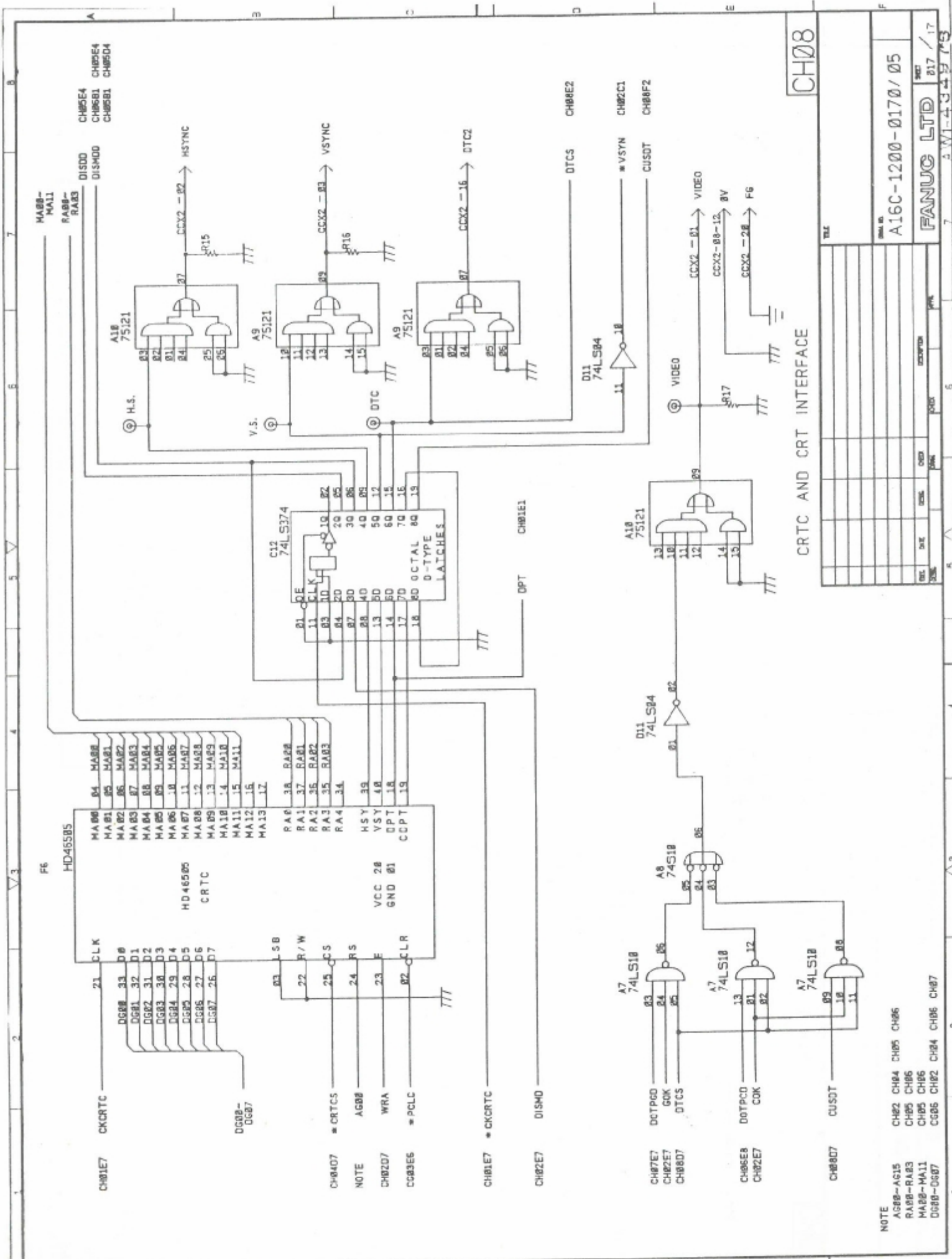
AWI-434973

FANUC LTD

A16C-1200-0170/05



CH05



CH08

CRTC AND CRT INTERFACE

REV	DATE	ISSUE	CHG	BY	CHK	APP	DESCRIPTION

REV. NO. A16C-1200-0170/05

FANUC LTD 017 / 17

NOTE
 AG88-AG15 CH82 CH84 CH85 CH86
 RA88-RA83 CH85 CH86
 MA88-MA11 CH85 CH86
 DG88-DG87 CG85 CH82 CH84 CH86 CH87